Further Analysis

In your analysis of the simulator you will want to experiment with varying the sizes of each of

the command line parameters to the simulator. You will also want to look at the dependence

between the di\_erent components in the system. For example you may want to ask questions

like (but not limited to) the following.

What happens when you vary the size of the Cache (between 256KB and 4MB) and TLB

(between 64 and 1024 entries)? Is there a relationship between the cache hit ratio and the TLB

hit ratio in this simulator?

What happens when you decrease or increase the amount of physical memory in the system?

For example, what happens when you set physical memory to 40 KB versus 2 GB?

Additionally be sure to include your responses to the analysis prompts posed elsewhere in

the assignment. When possible provide data and examples to assist your argument

What happens when you vary the size of the Cache (between 256KB and 4MB) ?

As the number of cache entries increase you reduce the number of misses in cache, this increases the Hit Ratio. Furthermore, as you increase the number of cache entries about the TLB entries you will not have hits to the TLB because they are already cached.

What happens when you vary the size of the TLB (between 64 and 1024 entries)?

As the number of TLB entries increase you reduce the number of misses in TLB, this increases the Hit Ratio. Furthermore, as you increase the number of TLB entries above what the cache is able to handle you will have more hits to the TLB.

What happens when you reduce the size of the physical memory (RAM)?

As the size of RAM is decreased you will have to go to disk more often. Time is increased drastically as going to disk is a lot more costly than RAM.

In your analysis, explain the di\_erences between the linear and 2-level page table imple-

mentations both conceptually and in terms of your implementation. Be sure to highlight the

advantages and disadvantages of each. Does the change from linear to 2-level have an impact

on the running time of this simulator? If so, how? If not, why? Does this change have an e\_ect

on the Cache, TLB, Swap, or Page Replacement Algorithm? If so, how? If not, why?

Differences between the linear and 2-level page table.

The linear simply takes the first 20 bits and indexes into the table. Whereas the 2-level page table uses the first 10 bits and indexes into the outer page to find the offset into the next 10 bits. This speeds up the process in finding the physical address. The main advantage is speed and you can use more memory. The running time of the simulator is slower in a two-level page table. Once the first 10 bits are indexed you have to find the next 10 so it is two lookups rather than one. Although it should be faster because you don’t have to look over a linear list. There should be no effect on the Cache, TLB, swap or page replacement algorithms. The page replacement algorithms effect RAM. The cache and TLB come before the page lookup so it does not effect that.